What is claimed is:

1. A semiconductor memory device, comprising:

a substrate;

a first semiconductor layer of a first conduction type having a single crystalline structure isolated from said substrate by an insulator layer;

a plurality of memory transistors, each having

a gate electrode connected to a word line,

a pair of impurity regions of a second conduction type serving as a drain region and a source region formed in said first semiconductor layer, and

a channel body of said first conduction type formed in said first semiconductor layer between said impurity regions, said memory transistors being operative to store data as a state of majority carriers accumulated in said channel body;

a plurality of device isolation regions formed to isolate memory transistors having gate electrodes commonly connected to the same word line from each other among said plurality of memory transistors; and

a plurality of impurity region isolation regions formed to isolate adjacent drain regions from each other and adjacent source regions from each other, said impurity region isolation region having a smaller width than that of said device isolation region.

2. The semiconductor memory device according to claim 1, further comprising:

a plurality of sidewalls each formed on a side of said gate electrode;

a silicide formed on said impurity region and extended to the location of said sidewall; and

a plurality of drain plugs each consisting only of a metallic material and connected to said drain region.

3. The semiconductor memory device according to claim 2, wherein said drain plug spans and commonly connects to adjacent drain regions.

4. The semiconductor memory device according to claim 1, further comprising:

a plurality of sidewalls each formed on a side of said gate electrode; and

a second semiconductor layer of said second conduction type formed in contact with and extended on said impurity region to the location of said sidewall.

5. The semiconductor memory device according to claim 4, wherein said second semiconductor layer has a higher impurity concentration of said second conduction type than that of said impurity region.

6. The semiconductor memory device according to claim 1, further comprising:

a plurality of sidewalls each formed on a side of said gate electrode;

a second semiconductor layer of said second conduction type formed in contact with and extended on said impurity region to the location of said sidewall;

a silicide formed on said second semiconductor layer; and

a plurality of drain plugs each consisting only of a metallic material and connected to said silicide.

7. The semiconductor memory device according to claim 6, wherein on adjacent drain regions portions of said second semiconductor layer are continuous and portions of said silicide are continuous, and on adjacent source regions portions of said second semiconductor layer are continuous and portions of said silicide are continuous.

8. A semiconductor memory device, comprising:

a substrate;

a first semiconductor layer of a first conduction type having a single crystalline structure isolated from said substrate by an insulator layer;

a plurality of memory transistors, each having

a gate electrode connected to a word line,

a pair of impurity regions of a second conduction type serving as a drain region and a source region formed in said first semiconductor layer, and

a channel body of said first conduction type formed in said first semiconductor layer between said impurity regions, said memory transistors being operative to store data as a state of majority carriers accumulated in said channel body;

a plurality of sidewalls each formed on a side of said gate electrode; and

a second semiconductor layer of said second conduction type formed in contact with and extended on said impurity region to the location of said sidewall.

9. The semiconductor memory device according to claim 8, further comprising a plurality of device isolation regions formed to isolate memory transistors having gate electrodes commonly connected to the same word line from each other among said plurality of memory transistors,

wherein said device isolation region adjacent to said pair of impurity regions of said second conduction type has a larger height than that of said pair of impurity regions of said second conduction type.

10. The semiconductor memory device according to claim 8, further comprising a silicide formed on said second semiconductor layer.

11. The semiconductor memory device according to claim

8, further comprising:

a plurality of device isolation regions formed to isolate memory transistors having gate electrodes commonly connected to the same word line from each other among said plurality of memory transistors; and

a silicide formed on and in contact with said second semiconductor layer and extended on said device isolation region.

12. The semiconductor memory device according to claim 8, further comprising:

a plurality of device isolation regions formed to isolate memory transistors having gate electrodes commonly connected to the same word line from each other among said plurality of memory transistors; and

a silicide formed on said second semiconductor layer,

wherein said second semiconductor layer extends on said device isolation region.

13. The semiconductor memory device according to claim 8, wherein said sidewall has a structure consisting of films of silicon nitride, silicon oxide and silicon nitride sandwiched between said second semiconductor layer and said gate electrode.

14. The semiconductor memory device according to claim 8, wherein said second semiconductor layer has an end extending to beneath said sidewall.

15. A method of manufacturing a semiconductor memory device including a plurality of memory transistors each for storing data as a state of majority carriers accumulated in a channel body sandwiched between a drain region and a source region, said method comprising:

forming a plurality of device isolation regions separately from each other in a first semiconductor layer of a first conduction type having a single crystalline structure isolated from a substrate by an insulator layer, said first semiconductor

layer including said drain region, said source region and said channel body formed therein;

forming a gate insulator film in a region on said first semiconductor layer defined by said plurality of device isolation regions;

forming a plurality of word lines containing gate electrodes separately from each other on said gate insulator film as crossing said plurality of device isolation regions to arrange said plurality of memory transistors in matrix;

forming sidewalls on sides of said gate electrodes such that a distance between sidewalls located between said gate electrodes has a dimension smaller than a width of said device isolation region;

forming trenches each having a smaller width than said width of said device isolation region in said first semiconductor layer by self-alignment using said sidewall as a mask to selectively remove said first semiconductor layer such that one and the other region to be adjacent drain regions are isolated each other, and that one and the other region to be adjacent source regions are isolated each other; and

forming bit lines connected to said drain regions formed in said first semiconductor layer and source lines connected to said source regions.

16. The method according to claim 15, instead of the step of forming sidewalls and the step of forming trenches, comprising:

forming first sidewalls on sides of said gate electrodes;

forming a second semiconductor layer on said first semiconductor layer between said gate electrodes by selective epitaxial growth after formation of said first sidewalls;

forming second sidewalls on said second semiconductor layer adjacent to said first sidewalls such that a distance between second sidewalls located between said gate electrodes has a dimension smaller than a width of said device isolation region; and

forming trenches each having a smaller width than said width of said device isolation region in said second semiconductor layer and said first semiconductor layer by self-alignment using said second sidewall as a mask to selectively remove said second semiconductor layer and said first semiconductor layer such that one and the other region to be adjacent drain regions are isolated each other, and that one and the other region to be adjacent source regions are isolated each other.

17. The method according to claim 15, instead of the step of forming sidewalls and the step of forming trenches, comprising:

forming first sidewalls on sides of said gate electrodes such that a distance between first sidewalls located between said gate electrodes has a dimension smaller than a width of said device isolation region;

forming trenches each having a smaller width than said width of said device isolation region in said first semiconductor layer by self-alignment using said first sidewall as a mask to selectively remove said first semiconductor layer such that one and the other region to be adjacent drain regions are isolated each other, and that one and the other region to be adjacent source regions are isolated each other;

forming second sidewalls on sides of said gate electrodes such that a distance between second sidewalls located between said gate electrodes has a dimension larger than a width of said trench; and

forming a second semiconductor layer on said first semiconductor layer between said gate electrodes by selective epitaxial growth after formation of said second sidewalls.

18. The method according to claim 17, wherein the step of forming said second semiconductor layer is provided after said trenches are filled with a silicon nitride.

19. A method of manufacturing a semiconductor memory device including a plurality of memory transistors each for storing data as a state of majority carriers accumulated in a channel body sandwiched between a drain region and a source region, said method comprising:

forming a plurality of device isolation regions separately from each other in a first semiconductor layer of a first conduction type having a single crystalline structure isolated from a substrate by an insulator layer, said first semiconductor layer including said drain region, said source region and said channel body formed therein;

forming a gate insulator film in a region on said first semiconductor layer defined by said plurality of device isolation regions;

forming a plurality of word lines containing gate electrodes separately from each other on said gate insulator film as crossing said plurality of device isolation regions to arrange said plurality of memory transistors in matrix;

forming sidewalls on sides of said gate electrodes;

forming a second semiconductor layer on said first semiconductor layer between said gate electrodes by selective epitaxial growth after formation of said sidewalls; and

forming bit lines connected via said second semiconductor layer to said drain regions formed in said first semiconductor layer and source lines connected via said second semiconductor layer to said source regions formed in said first semiconductor layer.

20. The method according to claim 19, wherein the step of forming sidewalls includes:

forming a second insulator film over said first semiconductor layer to cover said gate electrode, said second insulator film composed of a different material from a first insulator film formed on a side of said gate electrode;

forming, on said second insulator film, said sidewall facing a side of said gate electrode via said first and second

insulator films; and

removing said second insulator from beneath said sidewalls,

wherein the step of forming a second semiconductor layer is provided for forming said second semiconductor layer on said first semiconductor layer between said sidewalls and below said sidewalls by selective epitaxial growth.